SiGe 43.2 Gb/s 4:1 Multiplexor and Clock Multiplier for OC-768 Fiber Communications

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Abstract – **We have developed a Clock Multiplying Unit and 4 to 1 Multiplexor (CMU/MUX 4:1) that operates up to 47Gb/s. The on board VCO is LC tuned and the output clock jitter is 6pspp. The eye diagram of the output is 400mV swing with rise and fall times of less than 9ps. This integrated circuit was processed in a 120GHz BICMOS 0.25um process. Power dissipation is only 1W for a chip area of 2mm^2.**

I. Introduction

The next generation of optical fiber communications will require transmission speeds of higher than 40Gb/s. The OC-768 Synchronous Optical Network (SONET) standard with Forward Error Correction (FEC) will run at 43.2 Gb/s. Since 10Gb/s has become so commonplace that it can be done in 0.18um Complementary Metal Oxide Semiconductor (CMOS) process, and companies are selling Serializer-Deserializer (SERDES) Intellectual Property for it, the 40Gb/s communications are just around the corner. The equipment necessary to develop and test this technology is here already, and is provided by multiple vendors.

Silicon Germanium (SiGe) Technology, with unity current gain frequency (Ft) of higher than 120GHz is perfect for this market, being integrated with CMOS on 8 inch wafers, at very high yields. By contrast, Indium Phosphide (InP) process cannot currently achieve the level of integration needed for a full 16:1 transceiver implementation, and this technology may be limited to niche test and instrumentation applications.

II. Outline

We will describe a 4 to 1 multiplexor (mux) with integrated clock multiplying unit (CMU) phase locked loop (PLL), which achieves 43.2 Gb/s operation with good 0.4V 'eye' opening and low 6pspp jitter. Four inputs at 10.8Gb/s (SONET OC-192 with FEC) are time multiplexed to the higher 43.2 Gb/s rate. A 2.7GHz or 675MHz reference is multiplied by the PLL to the half-frequency of 21.6GHz. The output is clocked and multiplexed by both levels of our very symmetric clock, to eliminate duty cycle related jitter. The CMU requires a single external capacitor, or RC network, for filtering. This integrated circuit was also produced without the PLL, for laboratory test use, where a high quality 21.6GHz synthesizer with very low jitter is available. The stand-alone 4:1 Mux jitter is less than 4pspp, limited by measurement accuracy. A companion 1:4 demultiplexor (demux) that also requires external clock was also developed for bit-error-rate (BER) testing of the multiplexor

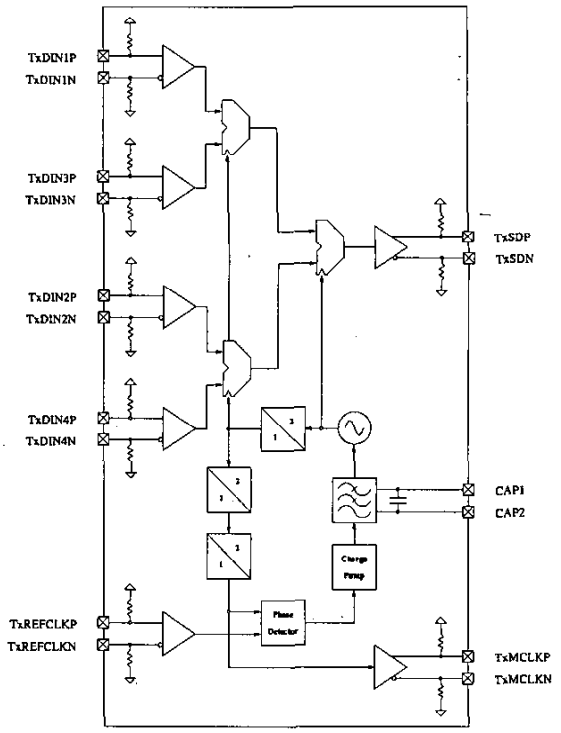

Fig. 1. CMU and MUX top level schematic

III. BLOCK DIAGRAM

All logic in our chip is done in full differential fashion. This has multiple benefits including: reduced voltage swing, phase margin tracking, noise cancellation, circuit simplification, etc. Figure 1 shows a top level

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interconnection of the main blocks in our circuit. All inputs and outputs are CML compatible; the inputs are terminated in 50-ohm load resistors.

IV. CMU

The on-board PLL takes either 675MHz or 2.7GHz into a digital quadricorrelator and locks a divided down 21.6GHz voltage controlled oscillator (VCO) to it. Locking is first achieved in frequency and next in phase. This phase detector has the advantage of being naturally multirate and also exhibits very low jitter. Other CMU implementations may show jitter that depends on the loop divider ratio and the amount of idle time between phase detector updates. Our loop bandwidth is higher than 10MHz, reducing incoming noise from the free-running VCO and rejecting crosstalk noise inside this bandwidth. See Figure 2 below.

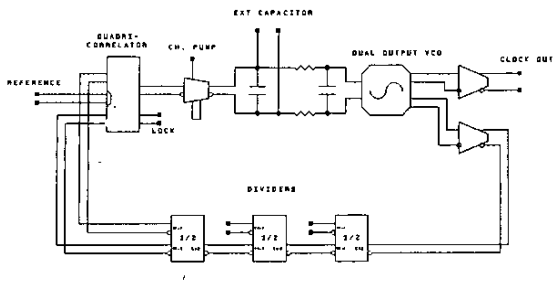

Fig. 2. The CMU is based on a digital quadri-correlator operating at 2.7/0.675GHz. The frequency acquisition circuit provides a lock detection signal.

V. VCO

A cross-coupled current mode logic (CML), or differential amplifier logic, forms the core of the negative resistance in the VCO (1). An LC tank is connected to the collectors of the amplifier and tuning is achieved by voltage control of variable capacitors (varactors). Our tank inductor is center tapped and a voltage lower than the VCC supply is applied at its center, as shown in Figure 3. This prevents forward biasing the emitter follower that buffer the differential outputs. Great care needs to be taken at 21.6GHz since the RC gain stages do not have enough gain to pass this frequency with ease. Inductive peaking can be used to increase the gain at these clock speeds. The number of emitter follower stages in series has to be kept to less than two because this IC works from 3.3V and also because too many of these stages in a row can cause undesirable signal growth.

VI. PHASE-FREQUENCY DETECTOR

The digital quadri-correlator requires two quadrature phases from the VCO (2). These are provided from the last divider, which has in-phase and quadrature (I and Q) outputs between its two latches in ring-divider connection. The reference clock samples the quadrature clocks that run at 2.7GHz and digital logic then determines relative frequency from the phase rotation of the beat frequencies that result. Next, phase is locked in a bang-bang or sign-only fashion by a sampling flip-flop.

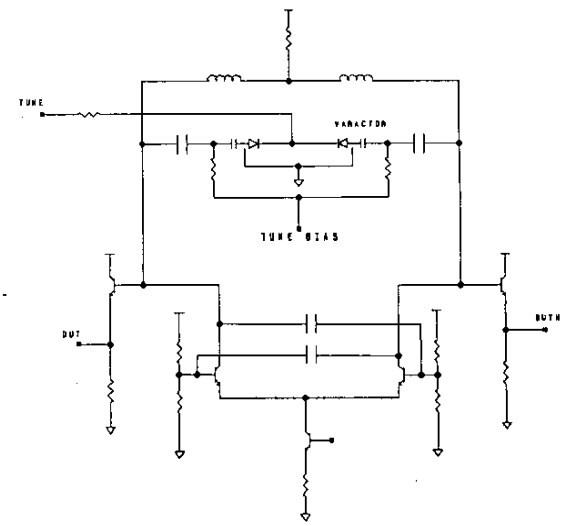

Fig. 3. The VCO is differential with varactor tuning. The voltage at the center of the tank is shifted to prevent saturating the emitter followers.

The only concern with a digital phase detector of this type is that the gain is very high and hard to predict. Gain can also vary a lot with temperature and process variations. In this application, there is no hard specification for the loop bandwidth, so making it wide enough for the jitter requirement was adequate. An alternative CMU in another IC that we developed uses the standard PFD that has predictable fixed gain, working comparably well for loop division ratio of 8.

VII. MULTIPLEXOR

Only one divider is required in the multiplexor since the output is clocked from the 21.6GHz VCO, and 10.8GHz is all that is needed in the first mux level. Care was taken to align the proper phase of the 10.8 GHz clock to the (final) 21.6GHz retiming. The difficulty with high-speed multiplexor design is that the data and clocks flow in

opposite directions. Clock centering needs to be done in Spice simulations.

Each 2:1 mux is composed of three latches and a 2:1 selector, as shown in Figure 4. When the top latch is holding, i.e. when clock is high, its output is multiplexed out; meanwhile the master latch of the bottom pair is holding the other input channel. When the clock switches, to low in this example, the data is transferred to the third latch and its output selected. The key to why this works well at high speeds is that the selection changes only when the input being selected is stable. No glitches can propagate in this arrangement due to causality.

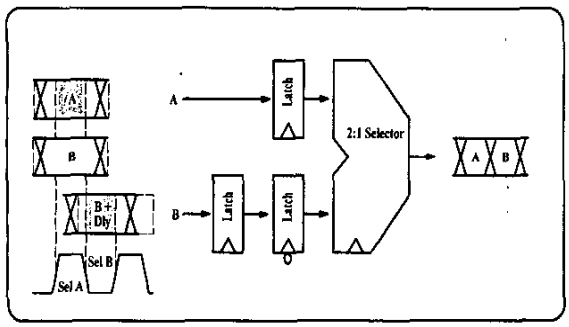

Fig. 4. Basic 2:1 Multiplexor consists of three latches and a 2 to 1 selector. Data is selected when it is stable.

VIII. TESTING

The IC measures 1x2 mm and is measured with a probe card consisting of high speed probes for the 2.7 GHz, 10.8/43.2Gb/s interfaces and DC needles with bypass capacitors for the remaining lines. Since equipment to test the OC-768 functions are extremely expensive (for example $US 1M for a complete BER test system) we developed auxiliary chips to allow us to do our own testing. We use a four-channel Pseudo Random Bit Sequence (PRBS) generator that works up to 12.5Gb/s. The electrical delay between channels is approximately 1/4 the PRBS length, avoiding artifacts of simultaneously driving each mux input with the same pattern. To simplify testing, each mux input is driven with a 250 mVpp single-ended signal via a DC block. Figure 5 shows the PRBS being driven with a 10.8GHz clock that is divided down to 2.7Ghz for the CMU reference input. Care needs to be taken that the mux inputs do not sample the incoming data during a transition; else the output of the mux eye will contain "sparkles". The output of the mux is monitored using a high speed sampling scope with a precision time-base that enables low jitter measurements and observation of waveform inter-symbol interference.

In addition to measuring the quality of the generated eye, we developed a 1:4 demultiplexor that is used with a companion PRBS decoder/error detector. The demux converts the 43.2Gb/s stream into four 10.8Gb/s data streams, any one of which can be feed into the error detector. The error detector uses an open loop design that avoids the need for a synchronization mechanism, requiring only a frequency counter to confirm error free operation. Again, care needs to be exercised when adjusting the phase of the demux and decoder clocks to avoid sampling during data transitions. Future designs will simplify the clocking of both the encoder and decoder portions of this test setup by integrating additional capability and eliminating the clock alignment nuisances.

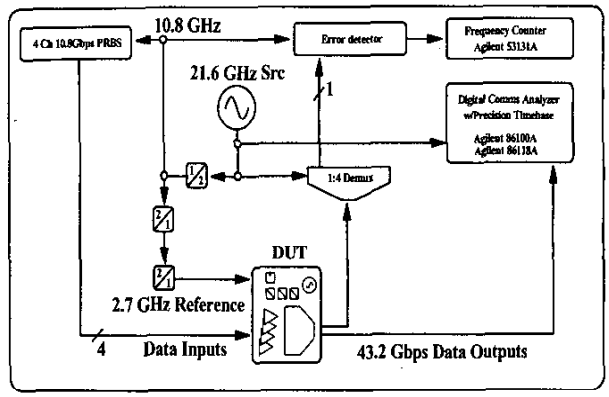

Fig. 5. Test Setup consists of a synthesizer, a PRBS source, an oscilloscope, a demux, a PRBS error detector and a frequency counter. 21.6GHz drives the demux and is divided down to provide the CMU reference.

IX. CHARACTERISTICS/MEASUREMENTS

Table 1 lists the main characteristics of the IC that generates a clear 400 mV eye amplitude with 1/6 pSrms/pSpp of jitter from a -3.3V supply drawing 300mA when operated at 43.2Gb/s. Measurements on static (DC) input data patterns show 0.25/2.2 pSrms/pSpp of jitter on the resulting output signal. Spectrum analyzer measurements @ 1 MHz offsets on the divided down VCO (2.7GHz monitor) show the noise to be better than -105 dBc/Hz. Both measurements suggest that the random component of the jitter is very small. The majority of the jitter is attributed to inter-symbol interference caused in part by the output stage and digital noise entering the VCO. Undershoot and "tram lines" on the edges of the eye diagram are indications of the ISI. At high temperatures (95C), the amplitude of the waveform decreased by ~10-15%, with little degradation of the jitter. The robust performance across temperature is due in part

to the use an LC tank; the variation in the oscillator's Kv was less than 10% over a 60C range.

Tuning Range	40-47 Gb/s
Locking Range	40-47 Gb/s
Eye height	> 400mVpp
Jitter:	1 pSrms, 6pSppk
Input Levels	> 200 mVpp (CML)
Input Return Loss	> 15 dB
Output Return Loss	> 15 dB to 30GHz, 10 dB beyond 30 GHz
Power Consumption	300mA at -3.3V
Temperature	0-75 C

Table 1: Basic characteristics of CMU-MUX

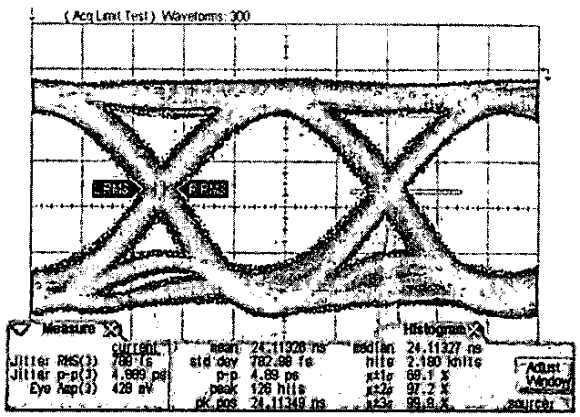

Fig. 5. Eye Diagram of 43.2 Gb/s output taken with high bandwidth head and low jitter trigger module.

X. PROCESS DESCRIPTION

The technology is a 0.25µm BiCMOS process with only 25 lithographic steps, offering 4 levels of Al and a full menu of active and passive devices. The process uses an essentially industry-standard, qualified CMOS platform, and offers two HBT devices with different speed/breakdown voltages by adding only 5 masks to the underlying CMOS process. The fast bipolar transistor's ft/fmax are 120/140GHz. Further key features are: 2.5V VDD MOS transistors for digital applications, including an isolated NMOS device for improved signal isolation; high-Q MOS varactors; two polysilicon resistors; a 2µm thick upper Al layer for high-Q inductor fabrication; and a 1fF/µm2 MIM [3].

The substrate resistivity is 50 ohm-cm., providing improved isolation compared to standard Silicon processes. The quality of spiral inductors also benefits from the lower substrate loss.

The process requires no trench isolation to achieve very high-speed performance. This is beneficial not only in cost and yield, but it lowers the self-heating of the bipolar transistors. Measured yields are very high and the IC's show very low Electrostatic Sensitivity Damage (ESD).

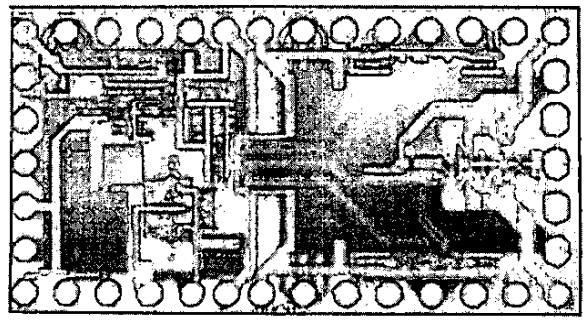

Fig. 6. Chip photograph of SiGe CMU-MUX shows PLL on the left side and MUX on the right. GSGSG outputs are on the right edge.

XI. ACKNOWLEDGEMENT

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XII. REFERENCES

[1] P.D. Capofreddi, et al, "A Clock and Data Recovery IC for Communications and Radar Applications," *IEEE Int. Workshop on Design of Mixed-Signal Integrated Circuits and Applications*, 1999, pp. 88-90.

[2] A. Pottbacker, U. Langmann and H. U. Schreiber, "A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s," *IEEE J. Solid-State Circuits*, Vol. 27, No. 12, December 1992, pp. 1747-1751.

[3] D. Knoll, B. Heinemann, K.E. Ehwald, H. Rücker, B. Tillack, W. Winkler, and P. Schley, "BiCMOS Integration of SiGe:C Heterojunction Bipolar Transistors," *2002 IEEE Bipolar/Bicmos Circuits and Technology Meeting Proceedings*, pp. 162-166.